Coarse Grain Power Gating in ASIC Designs Applications

Power gating, also known as Multi-threshold CMOS, is used to shut down certain power domains in a chip while leaving others active. Power shutdown can significantly reduce leakage power since many applications do not utilize all chip functions at all times. The basic idea of power gating is to separate the VDD or VSS power supply from the standard cells using power switches. The switches can be either PMOS or NMOS transistors that switch VDD or VSS, respectively. This talk focuses on coarse-grain power gating in ASIC designs, which switches entire blocks/rows of standard cells. This choice is due to lower cost and greater leakage savings of coarse-grain power gating compared to its fine-grain counterpart, which inserts the header or footer in each standard cell in the ASIC design library. More precisely, in my talk I will discuss and outline solutions.