Thursday, August 26th
Scaife Hall Auditorium
Room 125
4:30 p.m.
Refreshments at 4:00 p.m.

Massimo Alioto, Ph.D.
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Massimo Alioto (M’01–SM’07) was born in Brescia, Italy, in 1972. He received the laurea degree in Electronics Engineering and the Ph.D. degree in Electrical Engineering from the University of Catania (Italy) in 1997 and 2001, respectively.

In 2002, he joined the Dipartimento di Ingegneria dell’Informazione (DII) of the University of Siena as a Research Associate and in the same year as an Assistant Professor. He is the director of the Electronics Lab at University of Siena (site of Arezzo). Prof. Alioto is an IEEE Senior Member and a member of the HiPEAC Network of Excellence.

He is the Chair of the “VLSI Systems and Applications” Technical Committee of the IEEE Circuits and Systems Society, for which he is also Distinguished Lecturer. He is regularly invited to give talks and tutorials to academic institutions, conferences and companies throughout the world.

He has served as a member of various conference technical program committees (ISCAS, PATMOS, ICM, ICCD, CSIE) and Track Chair (ICECS, ISCAS, ICM, ICCD). He serves as Associate Editor of the *IEEE Transactions on VLSI Systems*, as well as of the *Microelectronics Journal*, the *Integration – The VLSI Journal*, the *Journal of Circuits, Systems, and Computers*, and the *Journal of Low Power Electronics and Applications*.

Ultra-low power logic circuits: from voltage-mode to current-mode

Abstract:

In the last few years, subthreshold VLSI circuits have become very popular in ultra-low power applications such as distributed sensing, wearable computing, biomedical devices, green electronics. These applications typically constrain the power budget to a few μWs and the supply voltage to a few hundreds of mV. Operation at such low power/voltage poses interesting problems and challenges, and at the same time offers new opportunities to develop emerging applications, as well as to stimulate and enable new technologies and markets.

In this talk, opportunities and challenges in the ultra-low power domain are presented. In particular, the degradation of the DC behavior of standard CMOS cells is discussed in depth for the first time, and practical voltage limits are derived consistently. Process/voltage/temperature variations and leakage are analyzed in a consistent framework to show how they ultimately affect voltage scaling and energy minimization. Other than exploring the energy/voltage boundary of subthreshold VLSI circuits, circuit design methodologies to push down the voltage lower bound in standard cell libraries are discussed. For the first time, robustness and yield are considered as further dimensions in the design space. In particular, the speech aims to clarify the important role (usually neglected) that the voltage lower bound plays in real VLSI circuits, and its relation with the optimal voltage that minimizes the energy consumption.

As an alternative approach to ultra-low power computing, MOS Current Mode Logic (MCML) circuits are explored as an alternative to standard voltage-mode CMOS logic styles. Design issues arising in the ultra-low power realm with a power consumption in the order of pW-per-gate are discussed, and appropriate circuit techniques to allow reliable operation are introduced.

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